Version with Markings to Show Changes Made

IN THE SPECIFICATION:

Please replace the paragraph that begins on column 3, line 47, with the following paragraph:

The voltage output of the converter is controlled by digital inputs on control input lines D0 through D5. The address input on these terminals address a read only memory 58, which provides a digital output as the input to the multiplying digital to analog converter (MDAC) 60. The analog output of the MDAC is provided as a positive input to a transconductance amplifier 62, the negative input to which is connected to the output voltage Vout. Thus, the transconductance amplifier 62 provides a current output proportional to the differential voltage input thereto with a gain set by external resistor Rgain, the differential input being the error between the output voltage Vout and the voltage commanded by the output of ROM 58 as a result of the digital input D0 through D5. The output current of transconductance amplifier 62 is provided to node 64, which is maintained at one Vbe above the 1.22 volt bias on the base of PNP transistor Q2. Also providing current to node 64 [62] is a current source I1, which is proportional to the target voltage divided by the input voltage V.

Please replace the paragraph that begins on column 7, line 8, with the following paragraph:

The negative input to comparators 80 and 82 is provided by the output of amplifier 68, which as previously described, provides an output proportional to the rate of change of the output voltage Vout, more specifically, an increasing output voltage for increasing rates in the drop of the output voltage Vout and a decreasing output voltage for increases in the rate of increase of the output voltage Vout. Assume for the moment that a large load is suddenly imposed on the converter, causing the output voltage Vout to begin to rapidly drop. This will drive the output of amplifier 68 sufficiently high to force the output of comparator 82, which is normally high, to go low. This forces the output of NAND gate 54 high, turning off n-channel power device N1 if it was on, and turning on p-channel power device P1, independent of the state of the respective pulse width modulator. Similarly, n-channel power device N2 will be turned off if it was on, and p-channel power device P2 [P1] will be turned on, independent of the state of that pulse width modulator. Of course, once the rate of drop of the output voltage Vout reduces, the output of comparator 82 will again go high, allowing the interleaved pulse width modulators to resume control of the output devices.

Please replace the paragraph that begins on column 7, line 50, with the following paragraph:

Also shown in FIG. 2 is a circuit for monitoring the error between the output of the MDAC and Vout, and for controllably reading the MDAC output. More specifically, the output of the MDAC and Vout are applied as the two inputs to window comparator 120, which provides a high output Voutok whenever the output voltage is within acceptable limits. This signal is applied as one input to NAND gate 122. The second input to NAND gate 122 is the input signal output-enable/shutdown OUTEN/SHDNB. When the output enable signal is low, the output of inverter 124 will be high, providing the shut down signal SHDN to shut down the rest of the circuit (the details of shut down circuitry in general are well known in the prior art and not part of the invention claimed herein). When the output enable signal is high, both inputs to NAND gate 122 will be high if the error signal is within acceptable limits, making the output of NAND gate 122 low, holding the output of AND gate 126 low and holding transistor Q16 off. Under these conditions, inverter 130 provides a high signal to the startup and overload circuit 22, indicating that the error signal is within acceptable limits. If the error signal moves out of acceptable limits, the signal Voutok will go low, driving the output of NAND gate 122 high. Since the

high state of the output enable signal is substantially equal to the analog voltage V, transistor Q7 will be off so that the resistor R18 [R16] will pull the input to inverter 134 low. This forces the second input to AND gate 126 high also, turning on transistor Q16 to indicate to the system connected thereto that the error signal between the commanded output voltage and the then existing output voltage is excessive.

Please replace the paragraph that begins on column 8, line 26, with the following paragraph:

The preferred embodiment of the present invention has been disclosed with respect to interleaved buck converters for purposes of specificity in the illustrative embodiment. The principles of the invention are not limited to such converters [inverters], however, and may also readily be adapted to boost or step up converters by one of ordinary skill in the art. Similarly, while a dual interleaved converter [inverter] has been disclosed, the principles of the invention may be applied to interleaved converters having more than two converters being interleaved. Thus while a certain exemplary embodiment has been described in detail and shown in the accompanying drawings, it is to be understood that such embodiment is merely illustrative of and not restrictive on the broad invention, and that this invention is not to be limited to the specific arrangements